SKA LFAA conceptual sub-rack design

Sub-rack proposal and main boards specifications

1 Document change log

Issue	Date	Change
1.0	05-10-17	First issue
1.1	11-12-17	Backplane Board specification update
1.2	18-01-18	Mechanical design update, general specification update

2 Definitions, Acronyms and Abbreviations

ADC	Analog to Digital Converter
ADU	Analog Digital Unit
AAVS1	Aperture Array Verification System 1
CPLD	Complex Programmable Logic Device
CPU	Central Processin Unit
DDR3	Double Data Rate 3 (memory)
DDR4	Double Data Rate 4 (memory)
EMC	Electromagnetic Compatibility
FPGA	Field Programmable Gate Array
INAF	Istituto Nazionale di astrofisica
IRA	Istituto di radioastronomia
iTPM	Italian Tile Processing Module
LFAA	Low Frequency Aperture Array
PCB	Printed Circuit Board
PPS	Pulse per second
PRE-ADU	Pre-Analog Digital Unit
RF	Radio Frequency
RFoF	Radio Frequency over Fiber
RMS	Root Mean Square
SKA	Square Kilometre Array
TPM	Tile Processing Module
VGA	Analog Gain Amplifier
WDM	Wavelength Division Multiplexing

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4 Scope

This document summarizes the sub-rack design activities conducted after the construction of the AAVS1 iTPM rack, aimed to meet LFAA requirements.
The design information coming from the field and from the activities involved in the deployment provides to the iTPM development group the basic specification to design a new electronic board by the AAVS1 lesson learned.
The starting points are to maintain the RF performance of the AAVS1 iTPM and to double the final rack density, to reduce the absorbed power and to simplify the rack design and complexity.
A complete integrated electronic, mechanic and thermal conceptual design is presented in this document.
All the objectives are matched and weighed specifications are produced to proceed with the next detailed design phase.

The design activities involve the groups that develop the AAVS1 iTPM with the collaboration of a new company, AAVID Thermalloy, specialized to design cooling systems.

This document is organized as follow:

- cabinet design elements, based on the proposed iTPM sub-rack elements
- design general criteria, adopted in the presented activities
- iTPM LFAA design update and specification
- iTPM sub-rack specification and design
- Sub-rack boards: backplane, management, ADU 1.5 board specification, main components and costs

5 Applicable documents

[AD1]	iTPM rev 1.2 user manual
[AD2]	

6 Reference documents

[RD1]	AAVID Thermalloy, Detailed Thermal Study Cooling Solution for SKA, BVE74 - Rev 5.pdf
[RD2]	AAVID Thermalloy, BG569 - CUSTOMER DESIGN DRAWING.PDF
[RD3]	AAVID Thermalloy, BLC69 - CUSTOMER DESIGN DRAWING.PDF
[RD4]	Leonardo Finmeccanica: TechnicalReport SKA LFAA Receiver.pdf
[RD5]	Samtec Fly Over product specification, fqsfp.pdf, www.samtec.com

7 Cabinet Overview

The SKA Low Frequency Aperture Array analogue chains deliver to a central processing facility and to the remote stations several thousands of optical fibers, each carrying two analog optical signals coming from the antennas installed in the desert area.

To acquire and process all these signals a special infrastructure will be provided for the central core and for the outer stations. Anyway, a common cabinet system for both locations will contain the acquisition electronics and the related functions, required for the LFAA.

Summarizing the main requirements needed for these infrastructures will be:

- iTPM boards are the basic element, receiving 32 signals each with 16 WDM receivers, standard 6U rack mount size.
- 256 single side cabinets containing 32 iTPMs each (8200 iTPM total)
- Clock distribution network from a single source to each cabinet with a 10 MHz and 1 PPS signals
- Control/data network based on 40G and 10G optical/copper (QSFP+) cabinet level links
- Three-phase 360V AC power supply
- 8°C water for liquid cooling to each cabinet

The cabinet design shall take account of several design criteria, general for a large installation and particular, related to the final destination location, in the middle of the Australian desert:

- Whole-of-Life Cost
- Energy Efficiency
- Capital Cost
- Reliability
- Maintenance

From the current iTPM 1.2 an updated iTPM 1.5 board design and a related compact and integrated sub-rack based solution are proposed for the LFAA cabinet, to meet all the LFAA requirements. The resulting rack design is a modular structure with function specialized components, summarized in Figure 1.

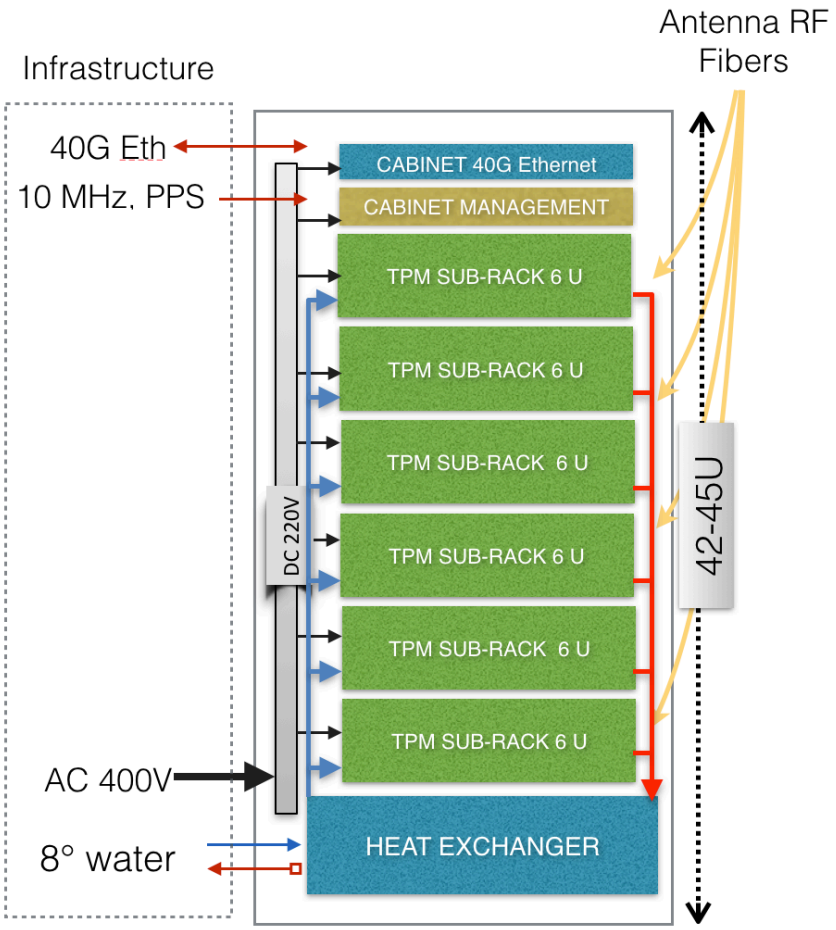


Figure 1. Proposed cabinet design with six (TBD) sub-racks for iTPM

The following elements are present:

- Heat exchanger and internal liquid cooling circuit
- A cabinet management board unit
- Four to six sub-racks containing 8 TPMs each, management board and supply unit
- 40G Ethernet switch
- AC Power distributor

The different sub-racks will integrate 8 iTPM boards each and all local management functions, like power, clocks and Ethernet.

Thanks to the functions and connections allocated to the sub-rack, the resulting cabinet level connections and cabling are simplified (Figure 2):

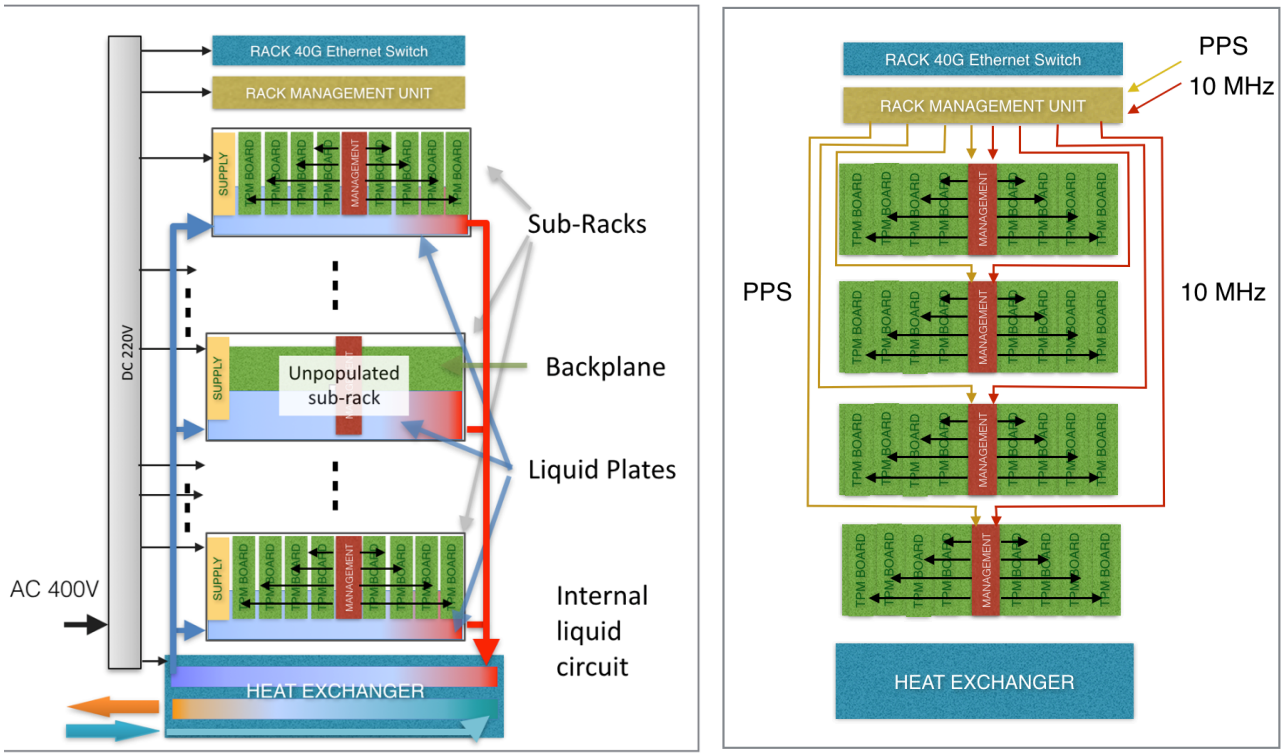


Figure 2. Heat, Supply and Management Ethernet and Synchronization signals

Furthermore this architecture simplifies the heat dissipation, and installation/maintenance.

The proposed cabinet will use standard cabling and mechanical interface to achieve a robust design and testability: that means each cabinet module can be fully tested as stand alone element.

The proposed subrack design should have the following general specifications:

- Standard 19" format, 6RU vertical spacing and 541mm horizontal depth
- liquid interface with about 10 lt/min at a maximum temperature of about 20°C (TBC, over the condensing temperature), from the rear part of the cabinet
- AC supply input with at least 1.2KW (220V or 360V)
- One reference and PPS clocks
- One copper gigabit Ethernet for management interface
- 16x8 RFoF for the iTPMs analog inputs
- 8 40G Ethernet interfaces for the iTPM data

7.1 Design General Criteria

The following listed issues and constrains have been considered as a driver to develop and design all the conceptual ideas of the systems presented in this document.

- The power consumption is critical, high efficiency is needed mainly for lifetime cost.
- Cabinet maximum height shall be less than 2000 mm from the floor (45 Rack Unit)
- Clock distribution network, 10MHz/PPS signals Jitter specification, signal integrity and isolation to guarantee overall system performances.
- Reduce the cost as much as possible
- Component availability for long time operating time shall be guaranteed.
- Each unit shall be Ethernet managed, directly or by the management board
- Connection of the cables available only front panel
- Minimum sub-rack density of 8 iTPMs and one management board.
- Easy testing
- Easy cabling and minimization of the front panel connectors
- Easy installation and maintenance
- Own power supply for each sub-rack
- EMC shielding

7.2 LFAA iTPM Design Update and Specification

The ADU board and the pre-ADU RFoF fiber interface board are the basic elements of the iTPM assembly.
Both boards are proposed as evolution of the AAVS1 design, with component update and new mechanical specification. The new iTPM version is identified as iTPM 1.5.
The LFAA rack density requirement is 32- iTPM (tentative 48), with the objective to increase the integration as much as possible, maintaining a reliable and cost-effective solution.
The first step to move in this direction has been a planar design to reduce the cabinet volume of the AAVS1 solution.
The second step was to move to a newer class of components on the ADU board, available for design and production with the current LFAA timeline in order to reduce the power consumption and heat dissipation.
FPGAs moves from the 20 nm based Xilinx Ultrascale to the 16 nm based Ultrascale+ devices; the ADC from the AD9680 to the equivalent device, power optimized AD9695; the memories from the DDR3 to the DDR4 family.
It has been also evaluated that high-level management functions, related to a CPU that can manage an operating system, can be efficiently executed by the proposed sub-rack management board and will be removed from the ADU. A simpler microcontroller unit will be placed in order to execute complex board level management functions. The telescope management application shall be specified accordingly.
Thanks to this evolution, the ADU board maintains the original architecture, increases the performance/resources and can reduce of about 20% the absorbed power.
Last but not least, a new iTPM 1.5 mechanical and interface connector layout has been identified to meet the sub-rack requirements to achieve the expected design density.

The new architecture solves several problems and allows a robust design for sub-rack level clock routing, thermal and mechanical interface. The proposed design allows to use standard 6U rack mechanical elements for the sub-rack structure, with reduced design effort and cost advantages.
The proposed approach provides a space inside the sub-rack structure for a power supply unit: The supply unit will be connected directly to the backplane to distribute the current to iTPM minimizing losses due to the cables routing.

The iTPM 1.5 preliminary layout is shown in Figure 3. Now, ADU and the PRE-ADU are in line. The ADU layout maintains the previous form factor with minor changes. The pre-ADU evolves greatly from AAVS1, to a single board unit with increased density. The preliminary pre-ADU board has been defined by Leonardo Finmeccanica design [REF4], but further improvement are still ongoing.

The ADU and the pre-ADU PCBs are proposed to be stand alone PCBs in order to reduce production costs. In fact, ADU board requires 14 layer structure with thousand of signals very

close to each other, against 2-4 layer PCB with reduced densities and only one supply, that pre-ADU requires.

In the ADU, to obtain the required signal impedance and isolation, a specific PCB build-up structure has been chosen, with a low dispersion dielectric material.

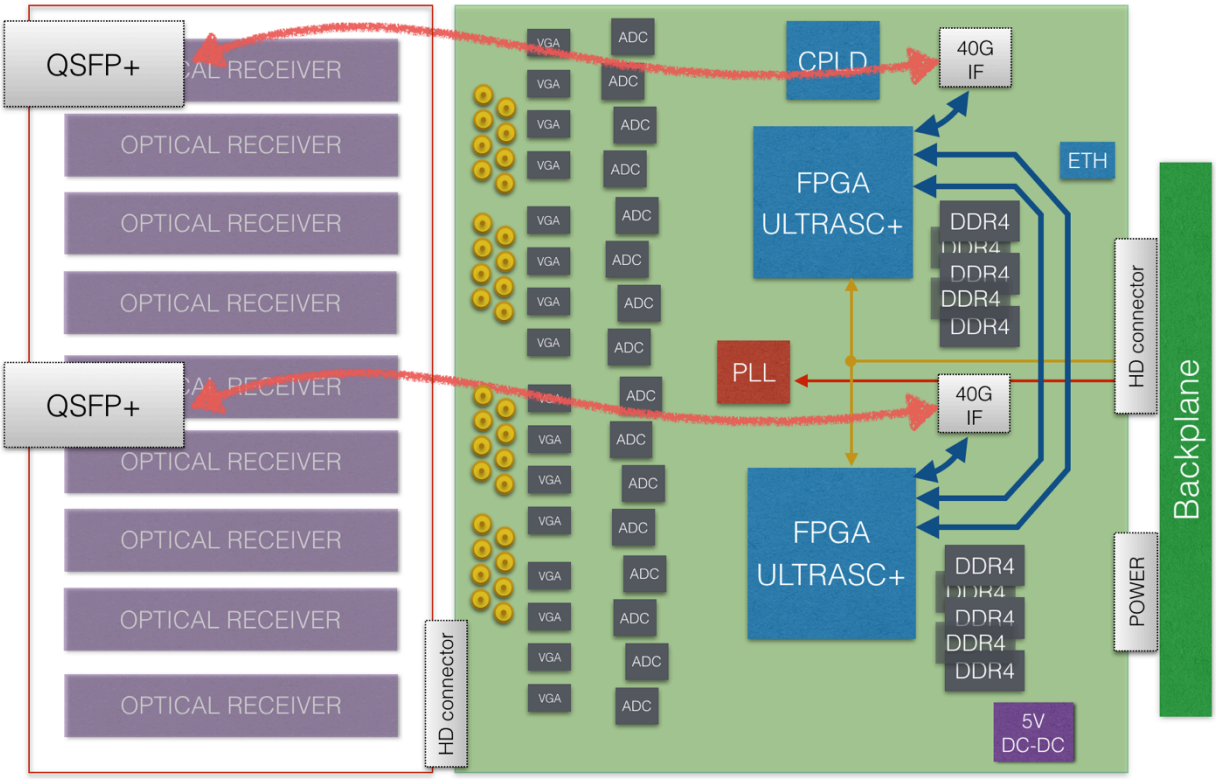


Figure 3. iTPM 1.5 preliminary architecture and layout

The 40G Ethernet interface shall be available from the sub-rack front panel; within the new mechanical specification this is achieved with the Samtec Fly Over products [RD5].

These new QSFP+ interfaces (available from 3Q 2017) have the capabilities of taking the 40G Ethernet signal from a PCB connector and placing the QSFP+ receptacle on a cable with panel mount configuration.

The 40G signals are sourced on the ADU close to the respective FPGA pins with the dedicated connector to the cables of a selectable length. On the other side of the cable the 40G QSFP+ mechanical interface can be placed on a separated PCB board, compatible with the required front panel mechanical specification. The related cable will be placed on the back side of the board, in order to minimize interferences with the optical receivers.

Excluding the RF analog output antenna signals and the 40G Ethernet, only some control signals and supply are needed by the pre-ADU from the ADU; the board interface requires a standard 14 pin board to board connector.
The RF analog outputs, coming from the optical receiver modules, are directly connected to the VGAs or passive ADCs inputs with single cable and micro-SMA interfaces (optional for test purpose).

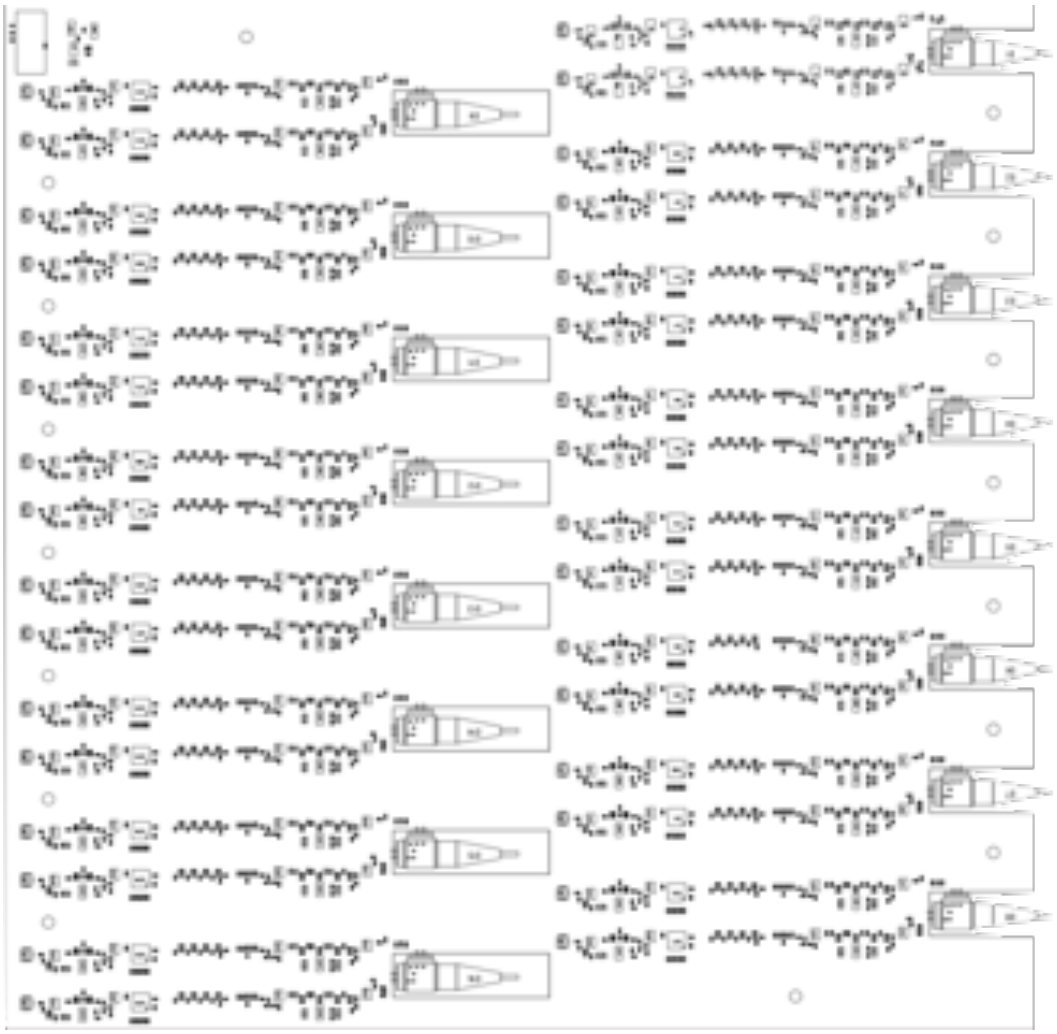


Figure 4 Preliminary PRE-ADU layout from feasibility study

Between the optical receiver and the RF analog front-end, RF accessible test points are available for production testing.

Summarizing, the main differences between 1.5 and the current release, 1.2, are:

- The ADU and PRE-ADU board interface is updated with new mechanical interface and new coaxial RF connector for each signal
- ADU and PRE-ADU planar configuration
- The ADCs are updated with the newer AD9695, reduced power equivalent version
- The FPGA family is updated to the newer one
- The CPU and his peripheral are changed to a simpler device
- The bus between the two FPGAs is moved to transceiver link, 4x or 8x doubling maximum transfer rate
- Coaxial connector RF input, optimized solution and integration with the PRE-ADU circuitry
- The DDR3L memories are updated to the DDR4 with different total size and byte organization; from 10 devices 2 Gbit with 16 bit output to 18 devices, 8 Gbit with 8 bit output for total capacity of 16 GByte + 2 GByte for parity check.
- Management and power connections are updated to the backplane interface
- Update in the power distribution systems for new board voltage and current settings
- The total size of the iTPM is updated to 233 x 445 mm

The usage of the new Analog Gain Amplifier (VGA), replacing the previous ADA 4961 shall be evaluated for the integration to the PRE-ADU in accordance with INAF, in the next generations of the board. As mentioned before, currently the design can allows to integrate them only for testing purpose.

The following table reports the detailed iTPM element power budget, moving from the AAVS1 iTPM ADU 1.2 to the proposed LFAA iTPM ADU 1.5. For the 1.5 versions two options are considered including a Low Power FPGA version and an updated low power PLL.

Peripheral \ Board Release	R 1.2	R 1.5	R1.5 option
Digital IC			
CPLD, Eth, Flash, …	3	2	
CPU	0,5	0	
FPGA, x2	55	52,0	40
DDR memories (*1)	3,4	5	
ANALOG (800 Mhz)			
PLL, CLKBuff, 10G Pll	3,6	3,6	1,6
ADC	52,6	25,1	
VGA		7,128	
FRONT END	16,7	10,6	
Power distribution efficiency:			
Digital:	90,25%		
Analog (150 mV linear drop):	82,1%		
TOTAL DIGIT IC, Watt:	68,6	65,4	52,1
TOTAL ANALOG IC, Watt:	68,4	43,6	41,2
Front End	18,5	11,7	11,7
TOTAL Supply, Watt:	**155,5**	**120,7**	**105,0**

(*1) The large memory array changes from a 2 GB DDR3L to a larger 16 GB DDR4, running at the same speed.

The main contribution to the power reduction is from the ADC converters that halve the absorbed power, without expected functional or performance changes.

The newest FPGAs are proposed in a standard configuration, with a reduced price or in a low power option with a considerable cost difference. Price difference is shown in the cost section of this document. About 12W of difference on each iTPM is expected.

The 120W LFAA iTPM has to be considered as nominal specification. The 105 W version can be considered as an option (with increased production cost).

8 Sub-Rack Specification

The sub-rack system is the basic structure required for the iTPM boards to be integrated. That element will provide all the accessories functions needed for a continuous iTPM operation inside the LFAA cabinet.
In order to simplify the rack cabling and design, the plan is to provide to the iTPM all the services that can be moved from the front-panel to the opposite side, with a backplane. The backplane design is not critical, in terms of connection density and signal speed.

Each sub-rack shall provide the following functions:

- Mechanical support for 8 iTPM boards
- Backplane to distribute to the iTPM Power, Gigabit management Ethernet, 10MHz clock and PPS
- Support the cooling at sub-rack level (air and liquid) for the iTPM and management boards
- Monitor each board absorbed current
- Power ON/OFF capability of each iTPM board (hot-swap if possible)
- CPU with Linux OS to manage high level operations
- Two Ethernet gigabit management
- Power Supply 220V AC (TBC)
- Easy access to the optical interfaces: the RFoF LC connectors are plugged on the front panel.
- Easy access to the 40G Ethernet QSFP cable: the QSFP cage are plugged on the front panel.

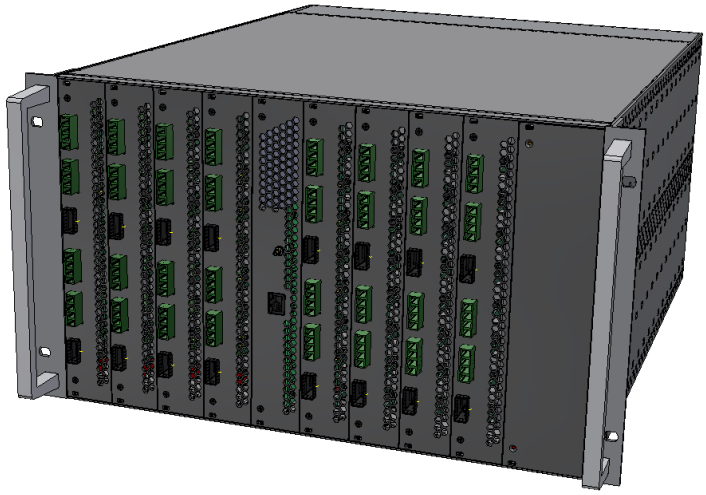


Figure 5. Sub-rack proposal with 8 iTPM, front view

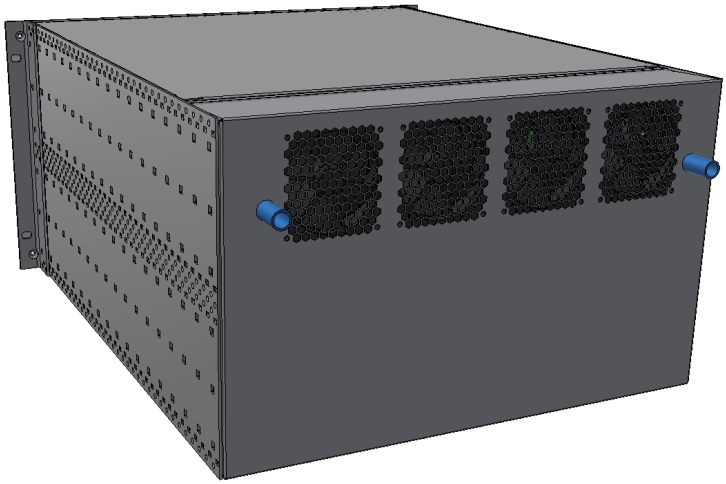


Figure 6 Sub-Rack proposal with 8 iTPM, rearview

The solution proposed is a 6U standard chassis with a custom backplane, a management board placed within the iTPMs, a power supply unit on one side and a liquid base cold plate system.
The Management board is placed in the center of the sub-rack and implements all the required functions needed to the iTPM to operate, including the power control, the distribution of clock signals and the gigabit connection. The Management can be remotely interfaced with a control application to execute cabinet-level operations, like iTPM configuration and monitoring.

iTPM and the Management are spaced with 8HP standard separation, corresponding to 40,64mm. A space of about 12HP, corresponding to 60,96mm on one side is available for a Power Supply unit.

The sub-rack concept incorporates mechanical and thermal design, built around the specification of the new iTPM.

Thermal design has been developed with the following thermal specification:

- each iTPM absorbs 120W
- FPGA, ADC and VGA components shall be directly cooled to the liquid with a junction temperature below 65°C to maintain optimal efficiency
- Air circulation will be forced from the front panel to the rear with four fans that work in extraction
- The air inside the sub-rack shall be maintained below 40°C, worst case

About the 75-80% of the dissipated heat will be directly transferred to the liquid circuit. Each iTPM will transfer to the circulating air about 20W.

The expected sub-rack power and thermal budget is summarized in the following table:

SUBRACK ELEMENTS	Element Watt	N°	Sub-rack Watt	Heat to Liquid, Watt	Heat to AIR, Watt
iTPM, (FPGA -1)	120	8	960	768	192
Management	30	1	30	0	30
Backplane	5	1	5	0	5
FAN	10	4	40	0	40
TOT, @ 12V DC:			1035		
Power Unit	62,1	1	62,1	0	62,1
TOT, @ 220V AC, 94% eff:			1.101	768	329,1
Options:					
iTPM FPGA -2L	-12	8	-96	-96	0
AC @360V AC, 96% eff:	-62,1	1	-62		
TOTAL OPTIONS:			-158		
TOT LFAA, 1025 Sub-racks, difference:			-162.053		

With the mentioned option of FPGA –L, the power absorbed from each iTPM is reduced of about 12Watt, that becomes 96 Watt for sub-rack.
The proposed 360V AC supply unit, with efficiency increased to 96% (TBC) reduced the power absorbed from the AC source of about 62 Watt.
The cost difference of the FPGA is available in a following section; the saving on power are under evaluation to be compared with the increase cost to the FPGA-L.

Sub-rack thermal design has been commissioned to the AAVID Thermalloy Company with the following elements and specifications:

- preliminary 6U sub-rack model, with detailed component 3D drawings, including internal board interfaces and backplane
- no active fans on the iTPM to obtain a robust design
- liquid circulation available for each sub-rack from the rear-side

- air circulation in each sub-rack shall be done with four fans placed on the rear side that extract fresh air from the front panel
- the iTPM board shall be removable for maintenance

The proposed solution is summarized in Figure 7 and Figure 8: two separate passive elements has been designed [RD1].

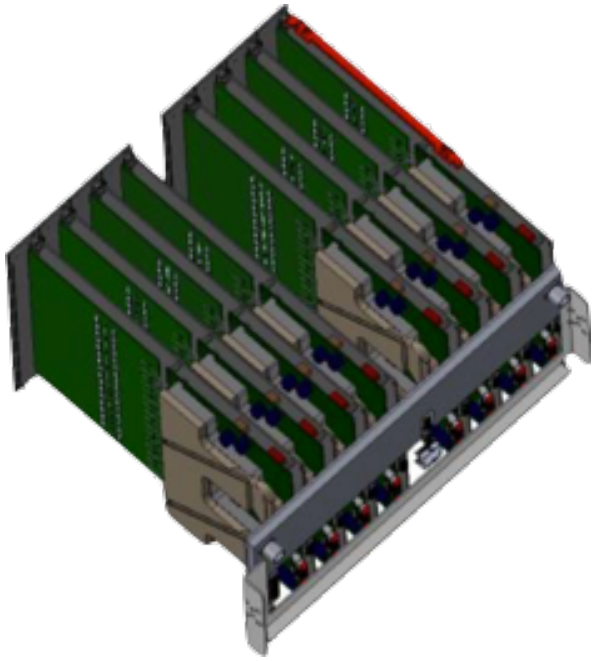


Figure 7 sub-rack cooling design

The main element is the heatpipe directly connect to ADU. It collects the active power and transport the heat to the rear part of the board to the backplane liquid plate by a special compressible thermal interface.
The second element is a liquid plate fixed on the backplane necessary to exchange the heat from the iTPM heat transport system to the cold liquid inside.

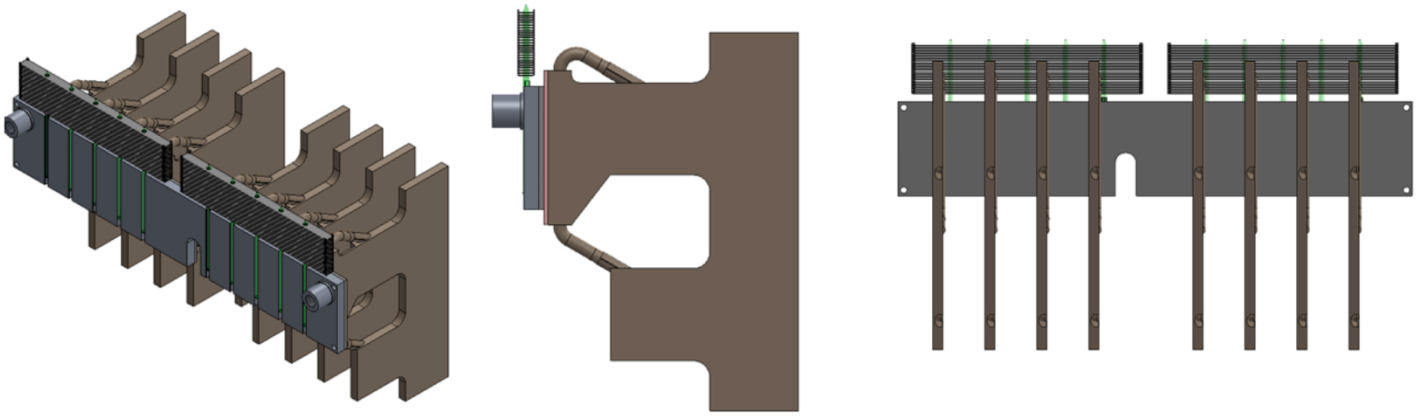


Figure 8 Sub-rack heat sink system, isometric view, TPM side view, rear view

The liquid plate interface also has some extruded heater for air-to-liquid cooling. This element will reduce the temperature of the air extracted from the sub-rack by small fans that will be placed behind and allows to maintain the temperature of the cabinet constant.

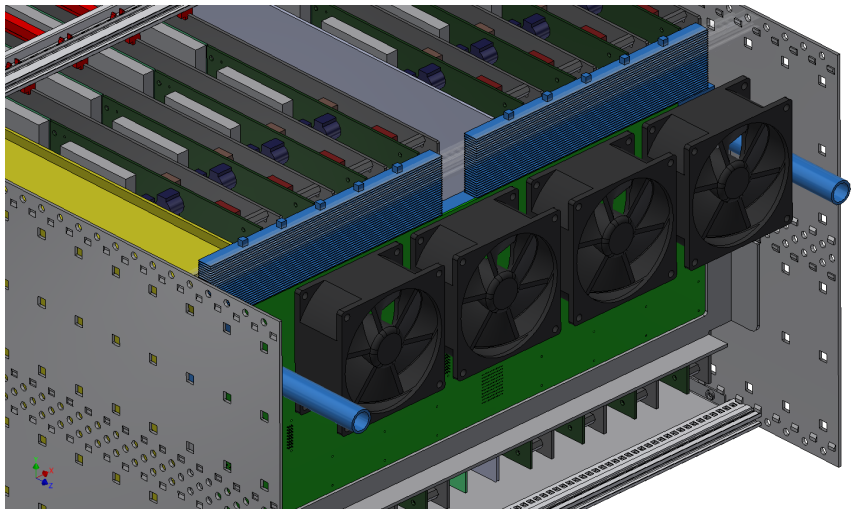


Figure 9 Air extraction and cooling design, elements

Four fans, placed on the external chassis, will create a low pressure zone in the volume comprised between the backplane and the rear part of the sub-rack.
Only the air extracted from the upper side of the backplane will be cooled and transferred to the outside internal rack volume. A proper natural air mixing is expected at rack level to receive a proper air temperature captured again from the sub-rack front panel (the cabinet is closed system).

The sub-rack management system will be able to control the fan speed, liquid plate temperature, board and air temperature at several points to define the internal temperature operative conditions.
Temperature working points shall be detailed with the final system power specification and design.

9 Sub-Rack Design

The sub-rack current design is based on four main elements: the mechanical 6U chassis with cooling, the backplane, the management board and the power supply.
This design has been conducted in strictly collaboration with INAF-IRA for the mechanics, AAVID Thermalloy for the cooling and by Sanitas EG for the electronic layout.

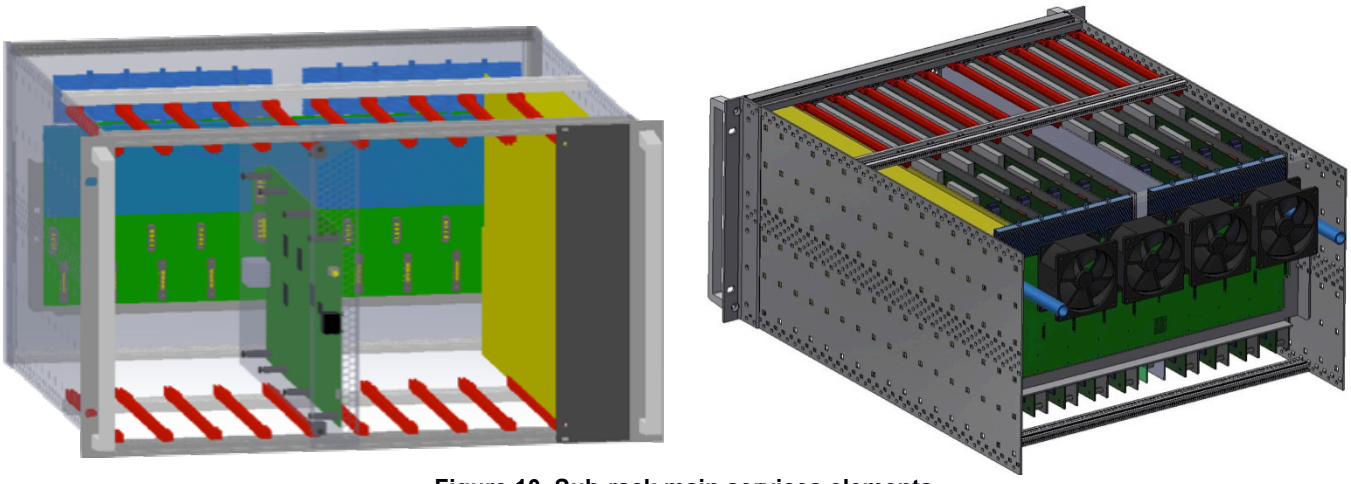


Figure 10. Sub-rack main services elements

The principal design characteristics considering the specifications needed and mentioned in the chapter before, are the following:

- 8 iTPM can be integrated in a standard 6U mechanical format
- a management board will be placed in the center of the sub-rack unit
- on a side, a power supply unit will interface with the cabinet supply and will power all the sub-rack functions
- a backplane board will provide the distribution of all the iTPM required services, including power distribution, clock distribution, management Ethernet distribution
- on the backplane a liquid cold plate will be integrated to allow the heat transfer directly from the iTPM heat sink to the LFAA heat transfer circuit
- the backplane liquid plate will provide also an air to liquid heat exchanger placed in the upper part of the backplane itself
- EMC shielding (conducted and radiated)

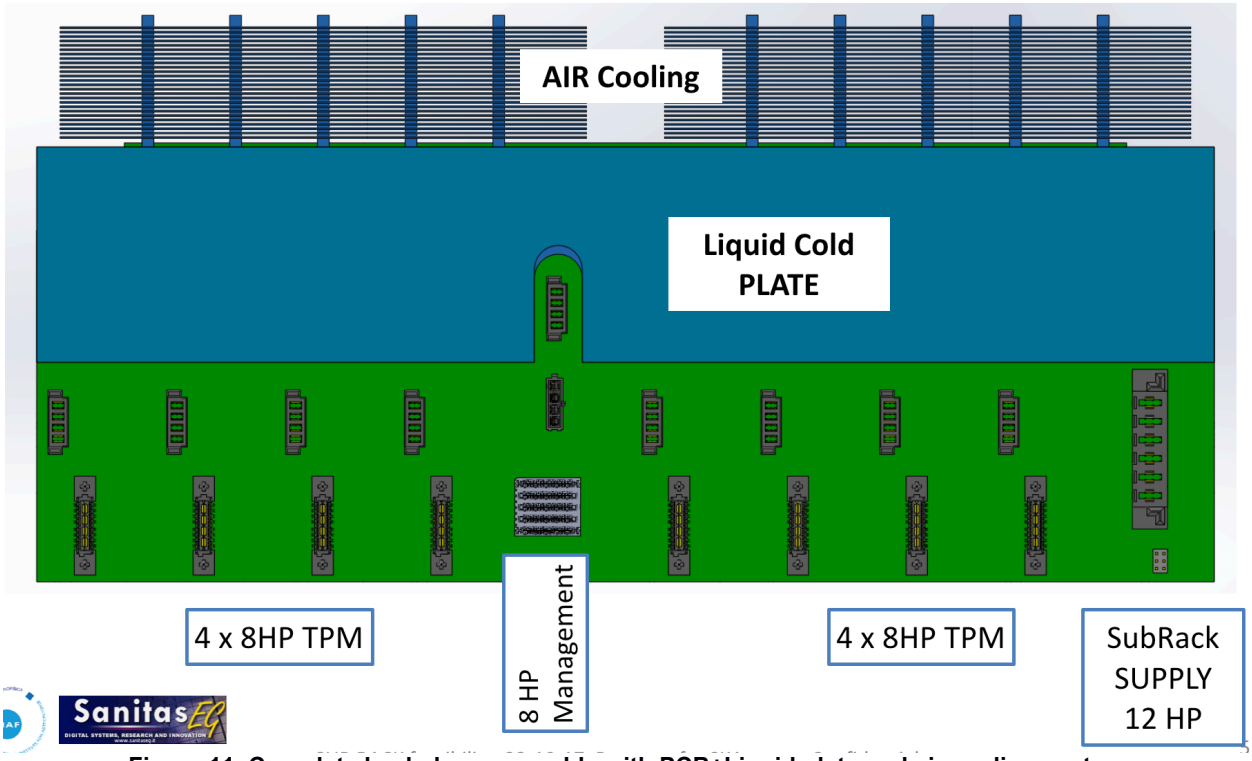


Figure 11. Complete backplane assembly with PCB+Liquid plate and air cooling system

The backplane provides the interfaces for all the sub-rack boards with exception of the 40G Ethernet and the RF fiber cables that are connected directly to each iTPM from front panel.
The PCB backplane is mechanically assembled with the liquid plate and fixed together to realize a single solidly element.
The PCB is organized in three areas (front view), from top to bottom: power & cooling, clock distribution, Ethernet and digital control interfaces.

The Liquid plate, main characteristics are the following:

- mechanical dimension defined accordingly the sub-rack proposed design and thermally dimensioned to sustain worst case sub-rack operative scenario
- planar interface for suitable heat transfer with heat-pipes
- valves for liquid directly accessible to the rear side of the sub-rack
- integrated air to liquid exchanger

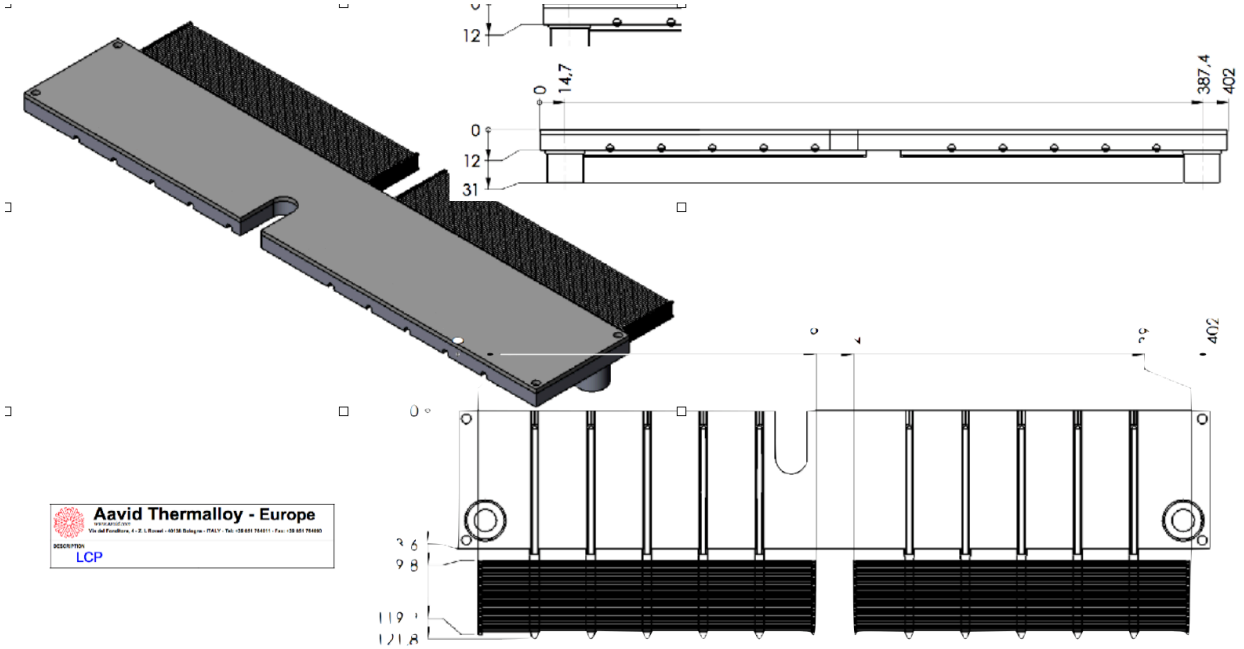


Figure 12. Liquid plate preliminary mechanical design

The liquid plate position is defined to optimize the efficiency of the iTPM heat pipe system, for the gravity effect. The interface connector between the iTPM and the backplane has been defined to avoid mechanical interferences between both.

Detailed design information is available in the design report directly provided by AAVID company [RD1], [RD3].

The LFAA iTPM heatpipe main characteristics are the following:

- Thin design, to increase density
- Remove heat from the FPGA, ADC and VGA devices, to cover about the 80% of the produced heat of the iTPM
- Only passive elements, to guarantee long lifetime and low maintenance
- Low cost

The proposed element is a heat-pipe based on aluminum plate that collect the power from the active device. The simple structure is shown in the following drawing.

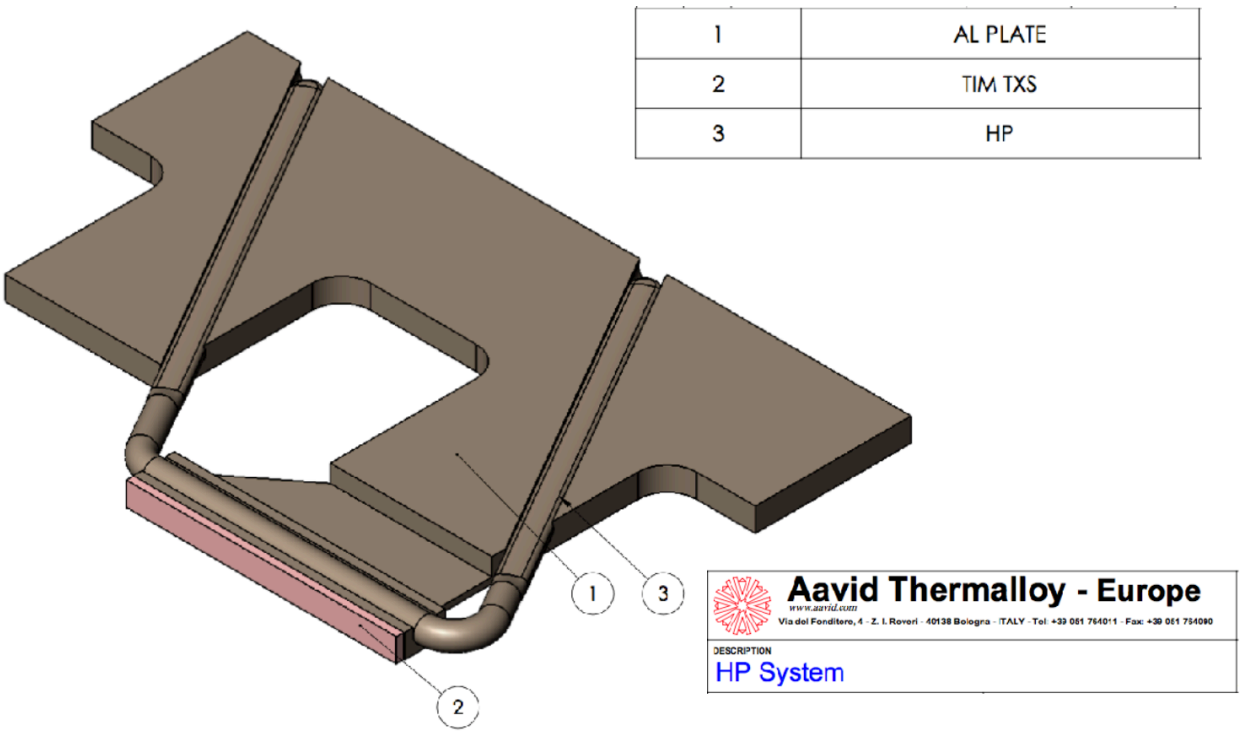


Figure 13. Heat pipe based ADU heat sink

The aluminum plate will be drilled and reworked in order to interface the electronic board to be hold directly to it. To manage the required tolerance between the iTPM board and the backplane, a thermal conductive soft thermal material will be placed on the interface (pink in the figure above, detail in the next paragraph and in [RD1]).

The ADU design specification has been updated accordingly in the new sub-rack structure and listed below:

- PRE-ADU interface connectors, both for RF inputs and control bus
- management interface connectors
- the mechanical factor has minor change due to the new heat pipe based heat sink, backplane connector specification and liquid plate interference

The resulting proposed layout is shown in Figure 14 and Figure 15.

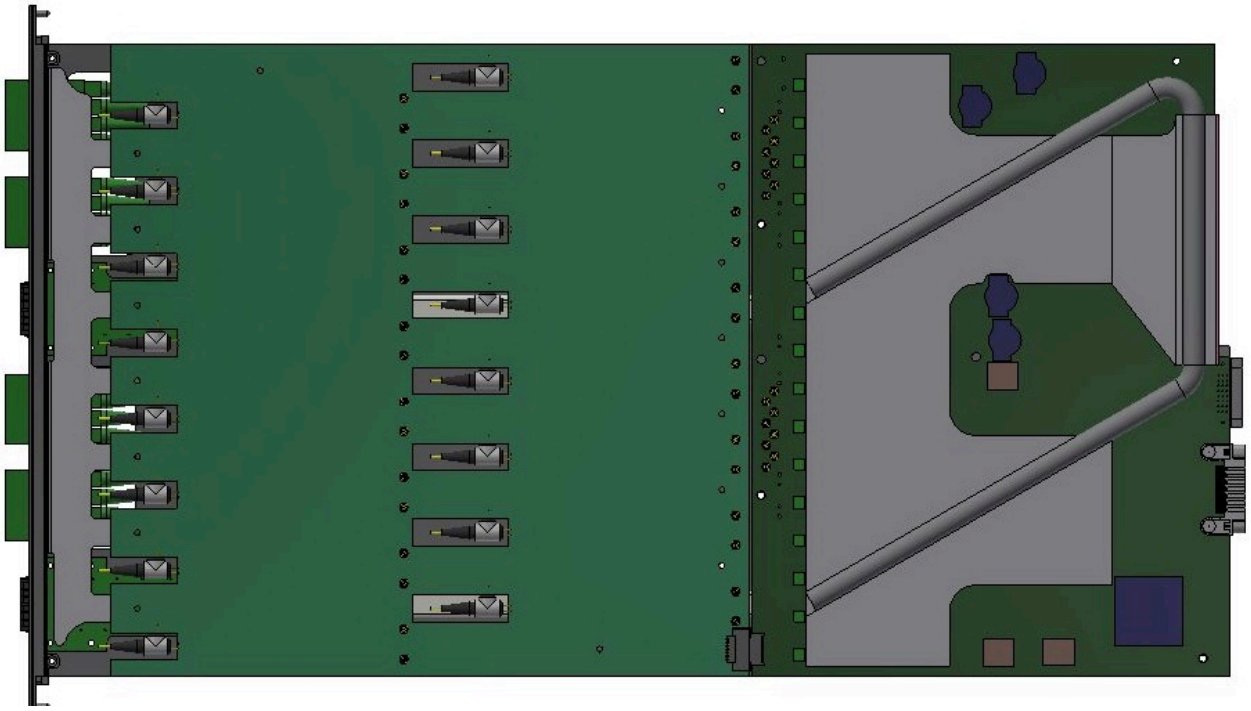


Figure 14. iTPM top view with the heatpipe system installed

The management connectors are grouped on the left, all the others main component positions are maintained as in the previous 1.2 revision.

The pre-ADU board has low power sparse component and does not require a heat transfer system. With the provided fresh air flow no special thermal design is requested.

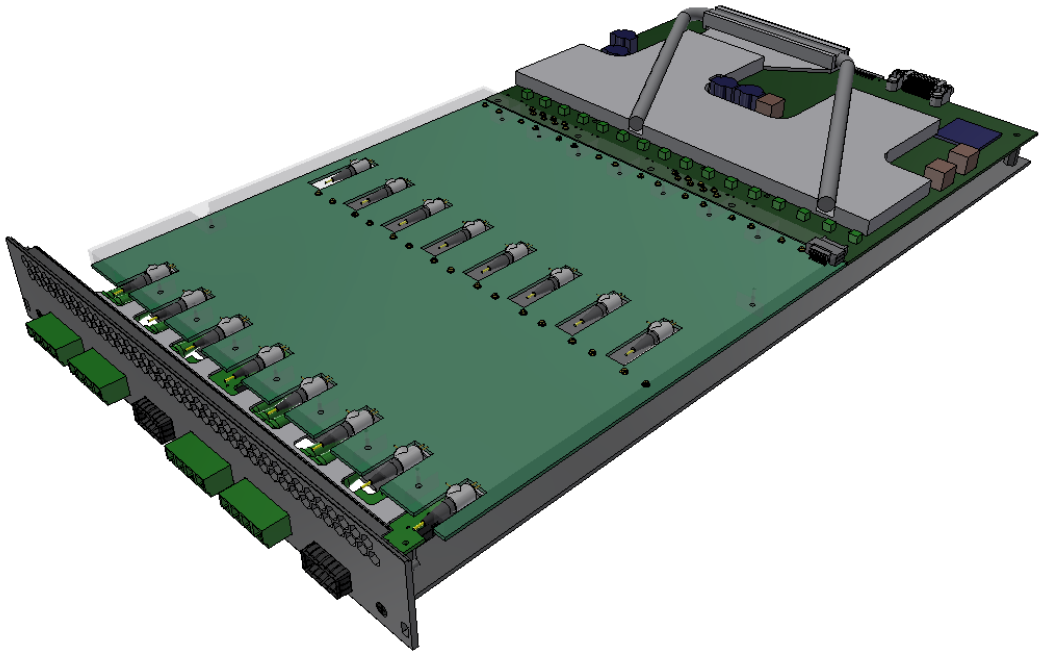


Figure 15. iTPM isometric view with metal plate supporting the boards

From preliminary thermal analysis, the system can be cooled down according with the specification of 65°C junction temperature, with an inlet water of 10 lt/min at 25°C of environmental temperature [RD1].

The management board does not require any heat sink system, because the dissipated power is low respect to the PCB dimension. The air flow that will be present in the sub-rack will be enough to guarantee a normal temperature of operation.

The internal mechanical integration of the tree principal electronics board of the sub-rack is shown in Figure 16
The backplane assembly will be fixed in the sub-rack chassis with robust interface to assure the required reliability and guarantee the mechanical tolerances.
The iTPM and the management boards will be inserted through the chassis guides (not showed) from the front and can be removed for maintenance.



Figure 16. Sub-rack main board integration

The liquid plate position is defined to optimize the efficiency of the iTPM heat pipe system, for the gravity effect.
The iTPM heat sink collects the heat coming from the ADC and FPGA to the heat pipe in the evaporating area. The heat pipe transfers the produced heat in the condensing area, corresponding to the liquid plate heat interface of each TPM to the backplane. It is expected that about 80% of the produced heat will be transported directly to the cabinet liquid circuit and the resulting power, generated by the remaining sparse and low power components will be transferred to the air flowing in the sub-rack.

The heat path is represented in the following Figure 17; the heat collected by the aluminum plate over the components generates the evaporation of the special liquid inside the heat pipe. The generated vapor will rise in these pipes to be condensed in the liquid plate heat transfer area. The condensed vapor will come back in the heat pipe structure to complete the required circulation.



Figure 17. TPM placement inside the sub-rack, heat path from main devices to the liquid plate

This technology allows to transfer up to 60W of power for each branch with a minimal temperature drop (normally 4-5°C are sufficient to make the circuit work).

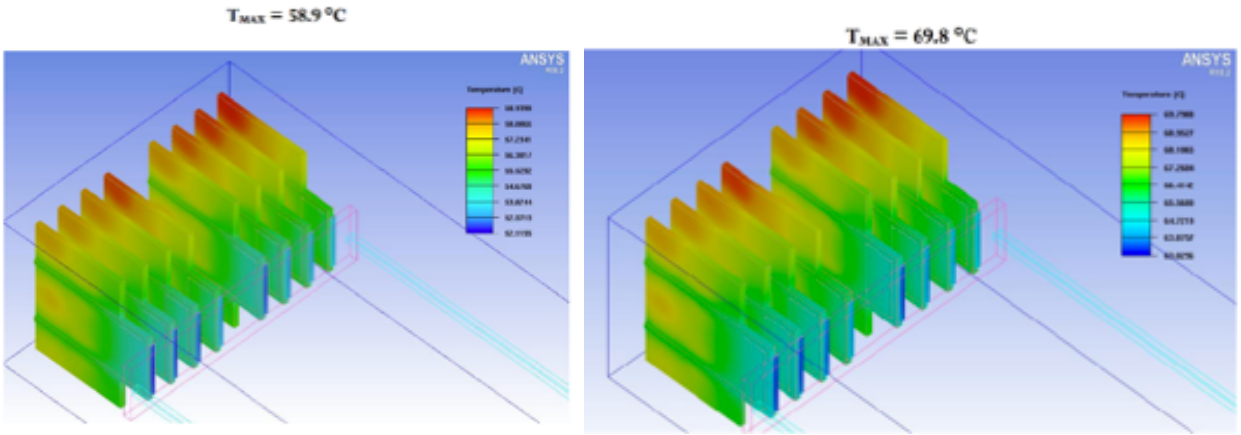


Figure 18. Thermal simulation with 1.0 & 1.5 thermal interface tichness

From AAVID simulation (Figure 18), it is evidenced that the overall efficiency is mainly dependent from the width of the gel pad required in the Heat interface between the iTPM and the backplane liquid plate. To meet the specification, maximum 1.5mm thickness gel pad shall

be used. Component maximum temperature has been evaluated with a 1.0 mm and 1.5 mm of soft thermal material, in a worst case scenario with 25°C of inlet water temperature (Figure 19).

SILICONE THICKNESS	T_{MAX} UNDER COMPONENT
[mm]	[°C]
1	53.9
1.5	68.9

Figure 19 Simulation maximum component temperature

From the thermal simulation comes also that the air to liquid heat sink of the liquid plate will reduce by about 8°C the temperature of the air extracted from the sub-rack.
The fresh air captured from the front panel passes through the iTPMs becoming hotter and then reaches the liquid plate. The liquid plate air exchanger cools the air, before reaching fans; then the air comes back to the cabinet internal volume.

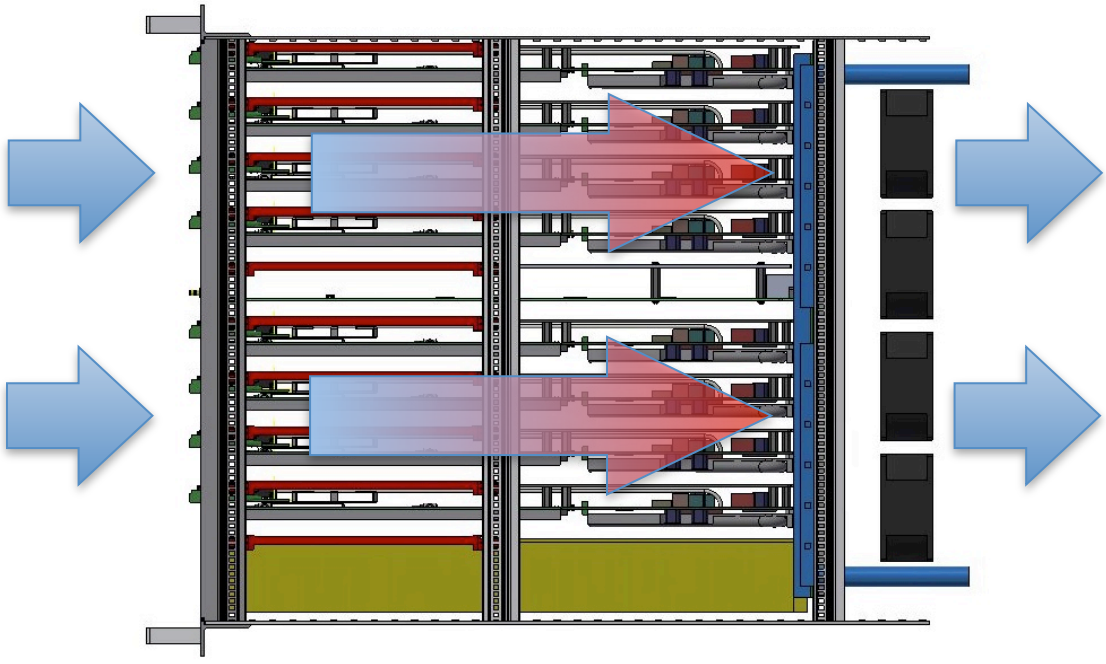


Figure 20. Sub-rack Top View with air extraction, fresh air from front panel

Adequate fans will be selected to obtain the required air flux and for the right temperature inside the rack. The effective air volume moved by the fans will be function of the selected cabinet internal liquid temperature and final iTPM power consumption.

10 Sub-Rack Boards

In the following sections the sub-rack electronic boards are described, with functional specification, preliminary component list and component cost for LFAA expected quantities.
The following boards are listed:

- sub-rack management board
- sub-rack backplane board
- iTPM ADU board

The information reported below shall be intended as specifications input for development.

10.1 Sub-Rack Management Board Specification

The sub-rack management functions are distributed between two boards (Management and Backplane).

The Management board supports all the high-level functions required to the iTPM to operate inside a large installation as required by the SKA LFAA telescope. The architecture and the functions allow high-level communication to a telescope manager application to control and configure, the iTPM and monitor all the heath function of the sub-rack. The same board integrates also the high quality reference clock distribution function and the gigabit switch to connect all the iTPMs to the Cabinet network.
The Management board takes from the backplane the main power, the synchronization signals and the management Ethernet link and distributes them to the iTPM through the backplane itself.
The power sourced from the backplane is managed by a protection circuit that measure the absorbed power and can be programmed for an automatic switch off if abnormal consumption occurs.
In normal condition the management board is always powered and execute the iTPM power ON and power OFF operations.

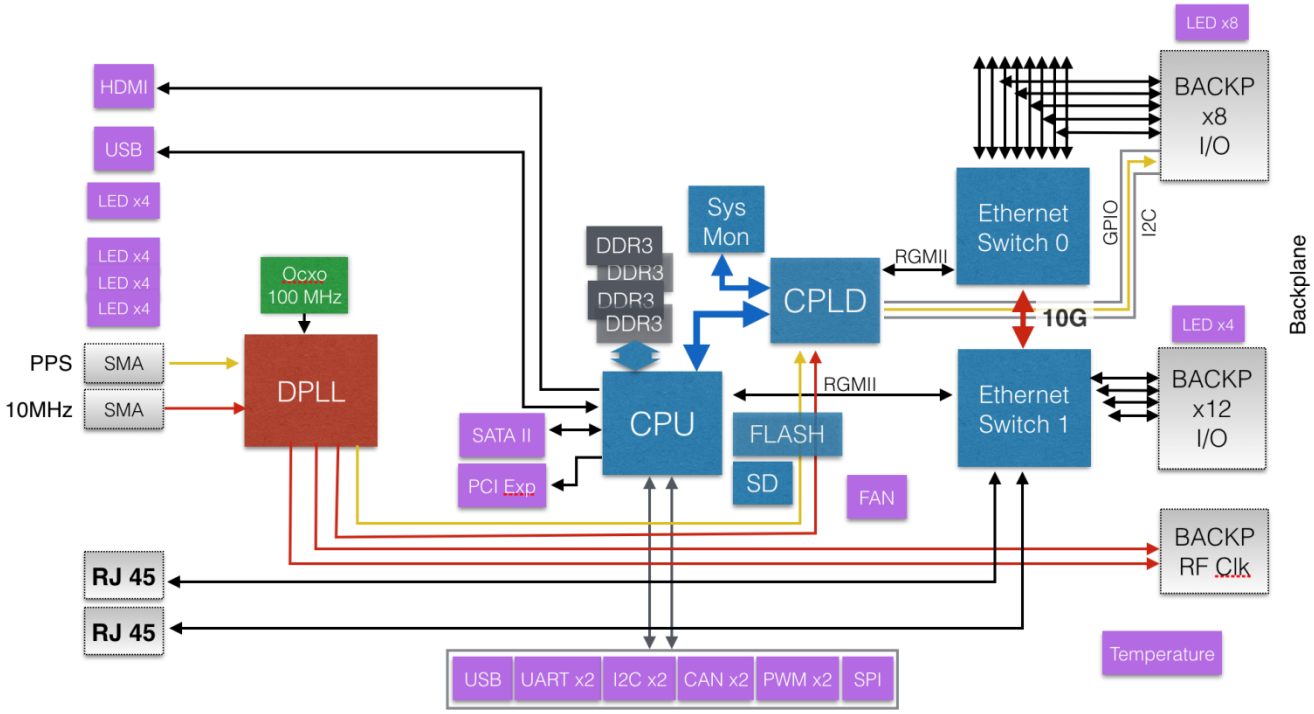


Figure 21. Sub-rack Management Board block diagram, preliminary

Sub-rack Management shall provide the following features:

SUPPLY

- Receive from the backplane the sub-rack DC supply from the main sub-rack supply unit
- Provide a protection circuit for overcurrent
- Manage the supply to the iTPM through the backplane, measure the total current, set the maximum load for each iTPM
- Provide the GPIO interface to the backplane to manage the single iTPM Power On/OFF and presence flag
- Detect the presence of the backplane
- Provide a I2C bus to control the active devices present on the backplane
- Provide the GPIO interface to the backplane to manage the single iTPM presence
- Provide the supply for the FAN, up to 2A, 12V. Alternative the power output shall be used as FAN power control if more power is required.
- guarantee deterministic power on sequence

CLOCKS DISTRIBUTION

- Receive the 10MHz clock from the front panel and distribute with minimum additive RMS Jitter to the backplane (2 signals, differential) and to local CPLD.
- Receive the 1 PPS from the front panel and distribute 2 PPS signals to the backplane.
- In alternative to the previous, with hardware soldering option, receive a 10MHz modulated with PPS, extract the cleaned 10MHz and the PPS and distribute them in the same way as previous
- Guarantee deterministic and equalized latency to the synchronization signal distribution, stable also in temperature
- Guarantee that the reconstructed PPS, if enabled, shall be synchronous with the 10MHz with a maximum RMS Jitter of 200 ps (TBC)
- Optical input to avoid self interferences by irradiation at the cabinet level

Ethernet

- Provide a 16 Gigabit switch with the following interfaces:
  - 2 Front panel RJ45
  - 8/12 Backplane link (to be defined the electrical specification, if magnetics are needed and where)
  - 1 RGMII interface to the CPU
  - 1 RGMII interface to the CPLD

CPU and CPLD

- Provide a low power, fan-less CPU with OS Linux support (32 bit, at least 600 MHz, single/dual core) with 512 MByte external memory, e-MMC boot flash and a SD card.
- The OS and the boot shall guarantee the maintainability
- Provide an instant-power-ON CPLD to manage all the power control signals and time sensitive signals. CPLD registers shall be memory mapped in the CPU
- Provide generic I/O and specific bus interface to connect sub-rack components, like temperature sensor, actuators, Voltage control for FAN, FAN speed sensor.

Mechanical

- Shall be compatible with the size of the iTPM, in order to have the position of the front panel and the backplane required for them.
- Shall guarantee an easy and safe connector for the Front Panel interfaces

User Interface

- Provide LED for status of the main functions of the management
- Provide LED to report presence detection of the TPM and signal defect device
- Provide Status of the cooling
- Provide Status of the total power delivered to the TPMs and the Power of each TPM

10.1.1 Management Board Component List

Description	Part Number	Pcs
Passive clock buffer	ADCLK946BCPZ	1
Active DPLL	AD9545BCPZ	1
OCXO	DOC102F-049.152M	1
TCXO	TB512-052.0M	1
CPU iMX6 ARM9 Dual 1Ghz	MCIMX6D5EYM10AD	1
CPLD	LCMXO3LF-9400E-6BG256C	1
MCU	ATSAM4S8CA-CU	1
CPU DDR3L MEMORY, 1GByte	MT41K128M16JT	4
CPU FLASH eMMC, 4 GByte	N2M400FDB311A3CE	1
CPU SPI FLASH MEMORY	M25P32	2
ETHERNET SWITCH	88E6390-A0-TLA2C000	2
ETHERNET MAGNETICS	TG111-S12NYN	8
Ethernet 10G	88X2222-B0-BKP2C000	1
Hot Swap controllers, power meter	LTC4281CUFD	1
Regulator	LTC4281CUFD#TRPBF	1
Regulator	LT8643SEV#PBF	2
Regulator	LTC3676	1
Regulator	LTC3374AEFE#PBF	1
RJ45	RJ45x2_Y_G	2
SMB conn	SMB5-J-P-HN-RA-TH1	2
Power Backplane	UPT-04-01-01-L-RA-LC-TR	1
Power Cabinet	PET-02-01-S-RA-LC	1
GPIO Backplane	EBTF-4-10-2.0-S-RA-1	1
Clock Backplane	IP5-04-01-L-S-RA1-TR	1
Led Pipe/column	Various	4
Inductors	Variuos, 74438357010	10
PCB	na	1

10.1.2 Management Board Costs

The main components have been quoted with SKA reserved prices. The price information is strictly confidential for the Xilinx and Analog items.
Following costs have been defined in accordance with the price scheme provided to us by INAF, detailed in Appendix A.

Description	Part Number	Pcs	COST, €
TOT HW costs			376,0 €
Labor & mechanical cost:			180,0 €
Cost detail:			
Passive clock buffer	ADCLK946BCPZ	1	3,8 €
Active DPLL	AD9545BCPZ	1	13,6 €
OCXO	DOC102F-049.152M	1	36,5 €
TCXO	TB512-052.0M	1	15,7 €
CPU iMX6 ARM9 Dual 1Ghz	MCIMX6D5EYM10AD	1	19,4 €
CPLD	LCMXO3LF-9400E-6BG256C	1	8,0 €
MCU	ATSAM4S8CA-CU	1	4,9 €
CPU DDR3L MEMORY, 1GByte	MT41K128M16JT	4	6,9 €
CPU FLASH eMMC, 4 GByte	N2M400FDB311A3CE	1	3,7 €
CPU SPI FLASH MEMORY	M25P32	2	1,5 €
ETHERNET SWITCH	88E6390-A0-TLA2C000	2	57,0 €
ETHERNET MAGNETICS	TG111-S12NYN	8	13,0 €
Ethernet 10G	88X2222-B0-BKP2C000	1	48,1 €
Hot Swap controllers, power meter	LTC4281CUFD	1	4,9 €
Regulator	LTC4281CUFD#TRPBF	1	4,8 €
Regulator	LT8643SEV#PBF	2	8,5 €
Regulator	LTC3676	1	6,4 €
Regulator	LTC3374AEFE#PBF	1	4,6 €
RJ45	RJ45x2_Y_G	2	11,2 €
SMB conn	SMB5-J-P-HN-RA-TH1	2	16,9 €
Power Backplane	UPT-04-01-01-L-RA-LC-TR	1	2,5 €

Description	Part Number	Pcs	COST, €
Power Cabinet	PET-02-01-S-RA-LC	1	2,0 €
GPIO Backplane	EBTF-4-10-2.0-S-RA-1	1	10,5 €
Clock Backplane	IP5-04-01-L-S-RA1-TR	1	7,3 €
Led Pipe/column	Various	4	5,5 €
Inductors	Variuos, 74438357010	10	13,9 €
PCB	na	1	40,9 € (1)
Estimated Labor and mechanics cost			
Mechanical		1	20,0€ (1)
Test			80,0€ (1)
Assembly			80,0€ (1)

(1) Preliminary estimation

The price is estimated with €/$ = 1,10, some parts have been quoted to SKA in USD$

10.2 Backplane Board Specification

The backplane is sited on the back of the sub-rack chassis and provides to each iTPM all the required power and services needed for SKA LFAA operations.

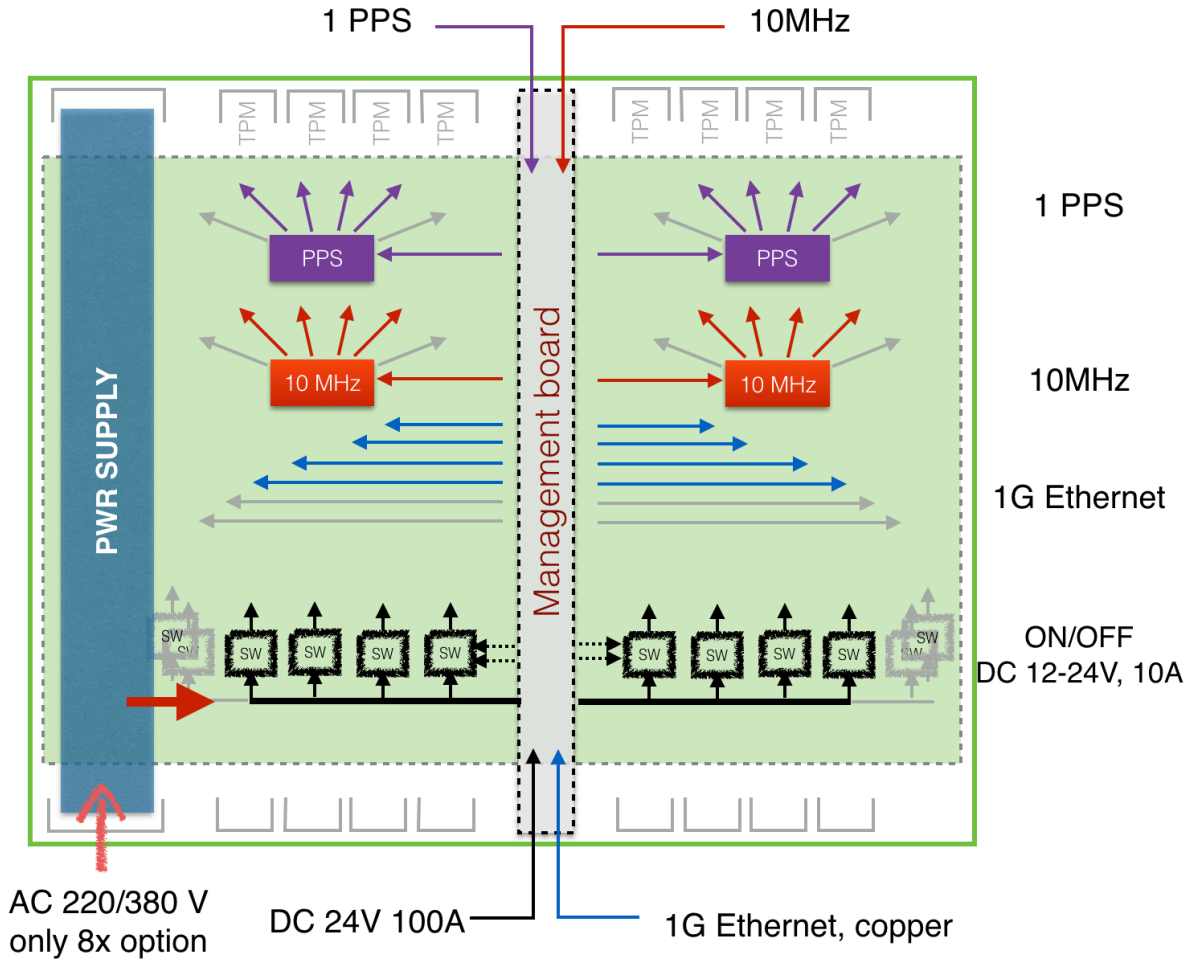


Figure 22. SUB-RACK Backplane block diagram

The backplane will interface directly with the liquid power plate, providing mechanical interface and temperature measurement in three different points, two under the liquid plate close to the liquid input and output pipes, one placed in the center to measure the temperature and humidity of the air circulating in the sub-rack .

The backplane provides the following functions:

- 8 slots for the iTPM boards, 1 slot for the management board
- a slot for a Power Supply inserted in the sub-rack with a power connector dimensioned to supply all the boards.

- Detect the presence of the iTPM
- Distribute the PPS to each iTPM (Two single ended signal coming from the management board shall be distributed to the iTPM)
- Distribute the two 10MHz clock to each iTPM with low RMS jitter..
- The PPS and Clock signal shall be equalized and length matched between them and between each iTPM
- Distribute the Gigabit Ethernet to each iTPM (4 differential traces, 100ohm matched for each iTPM)
- Distribute the DC power to each iTPM, measure the absorbed current, feature ON/OFF function sourced from the Management
- Monitor continuous power loading from each iTPM and perform automatic switch-OFF in case of extra-current
- Interface for 4 FANs with speed control and limitation of absorbed power/speed
- Two serial bus, I2C and One Wire bus, to all the iTPM for system configuration services
- Measure temperature in two different point of the board (liquid plate direct interface)
- Measure temperature and Humidity in one point of the board (ambient air interface)

10.2.1 Signals List

Backplane board specifications:

- 10 MHz RMS jitter contribute < 200 fs (tbc) with low insertion loss path
- 10 MHz isolation (vs all other signals) > 60 dB
- Power connector shall be capable to supply each TPM with 10A of maximum current
- Mechanical size shall be about 480x160 mm for the 8x version and 480x233 mm for the 12x version
- The PCB mechanical shall be designed in accordance with the sub-rack mechanical specification
- The Layout shall guarantee very low DC resistance for the power distribution bus from source to TPM, maximum 1 mOhm/m

The Management-Backplane signals list, in the x8 configuration, is the following:

Management-Backplane Signals	**Differential**	**Single Ended**	**Power**
Ethernet, differential	32		
10 MHZ, differential	2		
PPS		2	
I2C (SCL, SDA)		2	
iTPM Present		8	
Backplane Present		1	
FAN_RPM		4	
FAN_SUPPLY			1

The Management-Backplane additional signals list, in the x12 extension, is the following:

Management-Backplane Signals	**Differential**	**Single Ended**
Ethernet, differential	16	
TPM Present		4

The iTPM-Backplane signals list is the following:

iTPM-Backplane	**Differential**	**Single Ended**

Ethernet, differential	4	
10 MHZ, differential	1	
PPS, SE		1
iTPM Present/One Wire IF		1
iTPM RESET (*1)		1
iTPM GPIO (*1)		1
iTPM_PW_ALERT (*1)		1

(*1) These signals are managed by each iTPM Power Controller and shall be configured for function by the I2C interface

10.2.2 Backplane Board Component List

The component list for the Backplane is the following:

Description	Part Number	Number x8
Management Interface		
High Density Diff	EBTM-4-10-2.0-S-VT-1	1
RF clock	IJ5-04-05.0-L-S-1-TR	1
Power OUT	UPS-04-04.0-01-L-V-LC	1
iTPM Interface		
Power OUT	UPS-04-04.0-01-L-V-LC	8
Signals	QMS-016-06.75-L-D-DP-A-K-GP	8
Power Supply Interface		
DC in 3+3 AWG10	PET-06-01-S-VT-LC	1
Digital Interface	TBD (*1)	1
Power controller TPM	LTC4281CUFD	8
Clock & PPS distribution		
Clock buffer	ADCLK946	2
PPS buffer	CDCLVC1106PWR	2

Sensors		
Temperature sensor	ADT7408CCPZ	2
Temperature & Humidity sensor	HPP845E031R4	1
FAN interface		
PWM interface	PCA9530D,118	2
Standard 12V interface	Molex-47053-1000	4

10.2.3 Backplane Board Costs

The main components have been quoted with SKA reserved prices. The price information is strictly confidential for the Xilinx and Analog items.
Following costs have been defined in accordance with the price scheme provided to us by INAF, detailed in Appendix A

Description	Part Number	Pcs	COST, €
TOT HW costs, electronics parts:			246 €
Estimated Labor cost, preliminary			200 €
Cost detail:			
Passive clock buffer	ADCLK944BCPZ	2	6,9 €
Hot Swap controllers	LTC4281CUFD	8	38,8 €
Hot Swap MOSFET	various	8	7,3 €
High Density Diff	EBTM-4-10-2.0-S-VT-1	1	7,7 €
RF clock	IJ5-04-05.0-L-S-1-TR	1	5,3 €
Power OUT	UPS-04-04.0-01-L-V-LC	9	24,5 €
Other	Various	1	27,3 €
TPM signals	QMS-016-06.75-L-D-DP-A-K-GP	8	34,8 €
Power Supply Conn	PETC-04-12-04-01-S-VT	1	11,4 €
PCB	na	1	54,5 € (1)
Power Supply Adapter	Various	1	27,3 € (1)

Estimated Labor cost			
Test		1	120,0€
Assembly		1	80,0€

In the backplane several accessories and mechanical items shall be considered and added that overcome this feasibility study. Some elements are reported for completeness:

Description	Part Number	Pcs	COST, €
Estimated mechanical and cooling parts			
Chassis	24563-446	1	207,3 €
Mechanics, other	various	1	136,4 € (1)
Liquid Cold Plate	LCP BLC69	1	316,0€
Power Supply Unit, with redundancy	PET1300-12-054NA	2	661,8 € (1)

(1) Preliminary Estimation

The price is estimated with €/$ = 1,10, some parts have been quoted to SKA in USD$

10.3 ADU 1.5 Specification

Previous ADU board release (1.2) shall be updated to accomplish the new sub-rack specifications. New functional equivalent components are also proposed to reduce the absorbed power, increase the functionality and, if possible, reduce costs. High-level management functions have been transferred to the sub-rack management board and will be removed from the ADU.

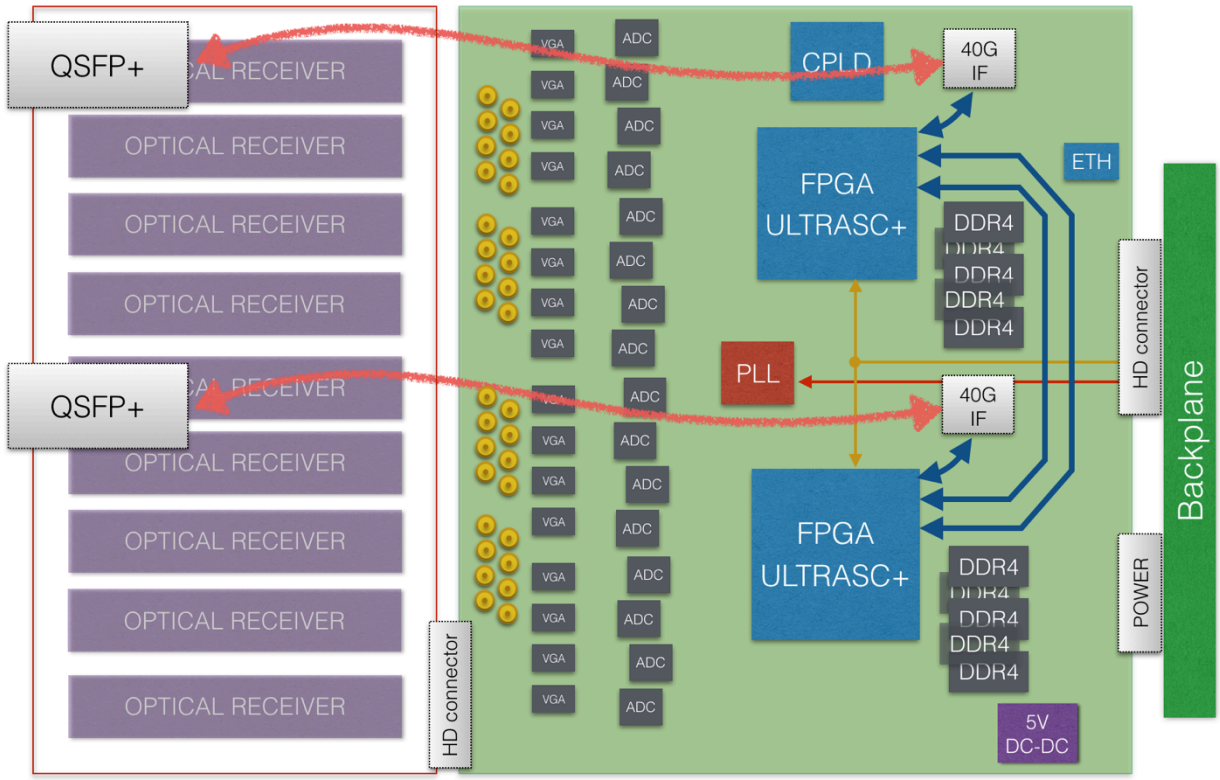


Figure 23. iTPM 1.5 preliminary architecture

The main differences between 1.5 and the current release 1.2 are:

- The ADU and PRE-ADU board interface is updated with new mechanical interface and new coaxial RF connector for each signal
- ADU and PRE-ADU planar configuration
- The ADC are updated with the newer AD9695, reduced power equivalent version
- The FPGA family is updated to the newer one
- The CPU and his peripheral are changed to a simpler device
- The bus between the two FPGA is moved to transceiver link, 4x or 8X doubling maximum transfer rate
- Coaxial connector RF input, optimized solution and integration with the PRE-ADU circuitry

- The DDR3L memories are updated to the DDR4 with different total size and byte organization; from 10 devices 2 Gbit with 16 bit output to 18 devices, 8 Gigabit with 8 bit output for total capacity of 16 GByte + 2 GByte for parity check.
- Management and power connections are updated to the backplane interface
- Update in the power distribution systems for new board voltage and current settings

The usage of the new Analog Gain Amplifier (VGA), replacing the previous ADA 4961 shall be evaluated for the integration to the PRE-ADU in accordance with INAF, in the next generations of the board.

10.3.1 ADU 1.5 Board Component List

The component list for the ADU 1.5 is the following:

Description	**Part Number**	**Number**	Company
FPGAs (*1)	XCKU9P-1FFVE900E	2	Xilinx
DDR4 Memories	MT40A1G8WE-075E IT	18	Micron
ADC	AD9695	16	Analog Devices
VGA	ADL5205ACPZ	16	Analog Devices
PLL	AD9528BCPZ	1	Analog Devices
Clock buffer	ADCLK948BCPZ	4	Analog Devices
CPLD	LCMXO3LF-9400E	1	Lattice
MCU	ATSAM4S8CA-CU	1	Microchip
QSFP+ Fly over	FQSFP–01–10.0–L–PF-2	2	Samtec
Backplane Interface			
Power IN	UPT-04-01-01-L-RA-LC-TR	1	Samtec
Signals & Clock	QFS-016-01-SL-D-DP-RA	1	Samtec
ADU Interface			
Power & Digital Control	SFM-107-02-L-DH-TR	1	Samtec
RF single connector	RSP-122811-01	32	Samtec

10.3.2 ADU 1.5 Board Costs

The main components have been quoted with SKA reserved prices. The price information is strictly confidential for the Xilinx and Analog items.
Following costs have been defined in accordance with the price scheme provided to us by INAF, detailed in Appendix A

Description	**Part Number**
TOT HW costs	***1.768,04 €***
Labor cost & IP cost:	***325,00 €***
Cost detail:	
Heat sink:	26,40 €
PCB	120,00 €
FPGA XCKU9P-1 **(*1)**	553 € CONFIDENTIAL
Analog, cumulative	567,00 € CONFIDENTIAL
DDR4, 16 GByte+Parity	157,50 €
DC-DC converters	50,00 €
Ethernet gigabit	8,00 €
Connectors	23,11 €
40G QSFP+ FLY OVER, 2x	68,30 €
CPLD & MCU	15,00 €
Other active	20,00 €
Passive components	160,00 €
Sanitas IP + Test bench:	200,00 €
Labor cost:	125,00 €

(1) The FPGAs listed are different for speed capabilities and power; the final selection shall be done based on the final design requirements. The price listed is referred to the standard device.

The price is estimated with €/$ = 1,10, some parts have been quoted to SKA in USD$

The different FPGA speed grade options and price, selectable for the iTPM-ADU 1.5 are the following, with corresponding SKA quotes:

Part Number	SKA quote, each	Pcs x board
XCKU9P-1FFVE900E	304,20 US$	2
XCKU9P-L1FFVE900I	426,19 US$	2
XCKU9P-L2FFVE900E	487,18 US$	2

The –L1 is a screened device that can work with 0,72V core with an expected power reduction for each FPGA from about 26W of the standard option to 20W, with 6W of reduction. The –L1 performance are reduced (the maximum speed of the FPGA element has been reduced to guarantee the functional specification with the lower supply voltage) with respect of the standard version and should be verified with a design implementation.
The –L2 option is a more restricted screening with the almost same performance of the standard version but the reduced power. The vendor proposes the selection with considerable difference in price.
The final choice shall be done in accordance with speed design requirement and balancing between initial costing and lifecycle costing.

11 Sub-rack Testability

The proposed sub-rack electronic board design has been conducted also following design for testability criteria.
The main testability elements that have been considered are the following:

- each sub-rack level function is implemented on a single hardware board
- standard board interface has been adopted, for internal and external connections
- power monitor has been provided for each board
- temperature sensors are present in several points
- all the relevant internal supply voltages are monitored

The proposed iTPM 1.5 maintains the previous testability capabilities that include:

- high speed bus marginality check (eye diagram on the transceiver 10G buses, data valid windows measured on each internal gigabit bus line)
- FPGA configuration memory monitoring and scrubbing
- acquisition chain loopback capabilities and test pattern generation capabilities

A production and assembly test plan can be defined with 100% of functional and performance coverage.
Production test information for each board can be stored in a database for further reference.

Some on-line monitoring and test functions can be executed during the telescope operations and also off-line diagnostic operations can be loaded on-the-fly, in order to guide the further maintenance operations. Each sub-rack board shall be fully verified as stand alone element also in the LFAA site in order to minimize the overall maintenance cost.

12 Sub-rack Weight

The proposed sub-rack estimated weight, fully populated, is about 30 Kg.

The weight is calculated from the detailed 3D model assuming aluminum as the final material.

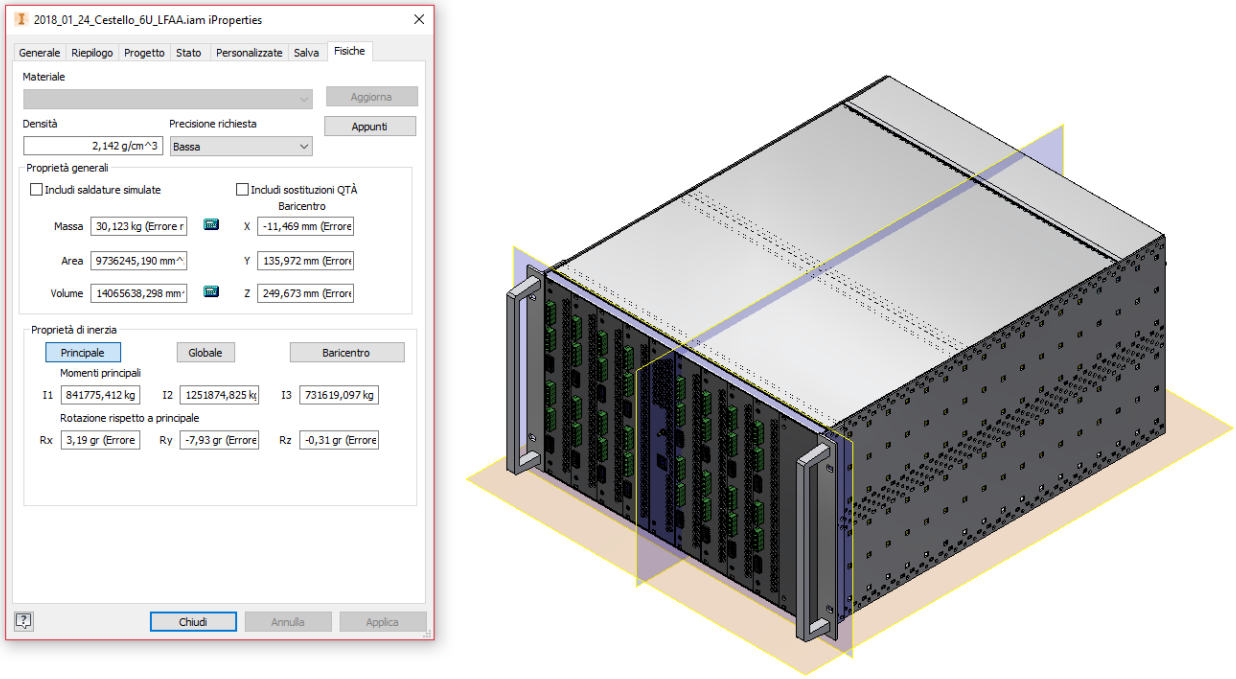


Figure 24 iTPM sub-rack mechanical model physical proprieties

It has been assumed that the supply unit weight will be 5 Kg.

In the design the iTPM boards can be safely inserted and removed. As consequence it can be evaluated the weight of the single complete iTPM and the rest of the sub-rack parts as possible stand alone elements of reduced weight.

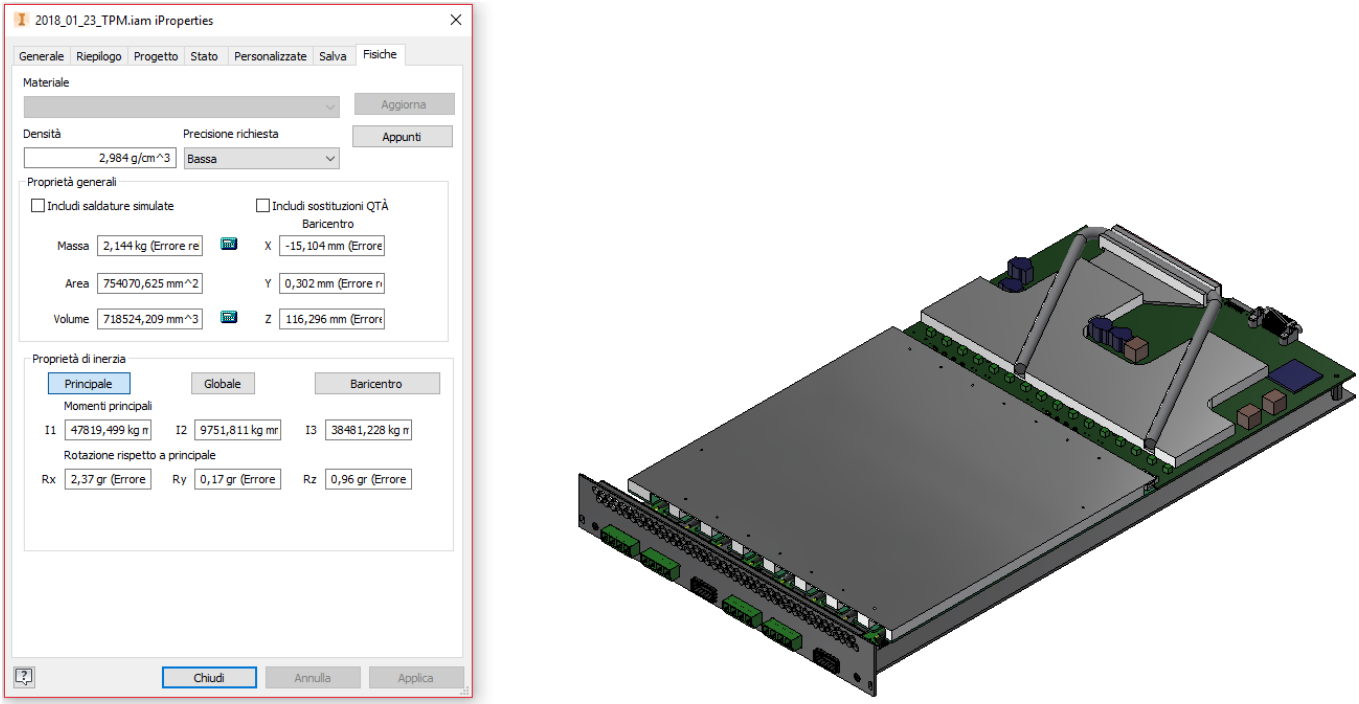


Figure 25 iTPM 1.5 estimated weight

The estimated weight of each TPM is about 2.15 Kg

The resulting unpopulated sub-rack, with supply, backplane and management become about 12,9 Kg.

APPENDIX A: SUBRACK COST

The Sub-rack cost are summarized considering the following cost structure:

- Hardware cost, based on current proposed design
- Labor cost, including assembling and testing

The test benches cost can be partially covered from the AAVS1 activities that need to be updated for the new system.
Other cost, related to services, financial charges, general cost and gross margin are not included.
Main part of the quoted device are in US$, the €/$ = 1,10 has been considered.

The Pre-ADU cost estimation comes from INAF quote, to a third party company.

The LFAA Projection is exposed for the single sub-rack elements and for the total LFAA budget, considering 10% of spare parts.
The Yellow cells stand for budgetary because not all design elements has been quoted but only estimated from similar design.

Part	LFAA Projection	LFAA Budget, 9000 TPMs, 1125 Subracks
Backplane, Chassis, Liq. Plate, Power Units	1.767 €	1.988.233 €
Management	556 €	625.502 €
TPM, ADU, 16GBYTE:	2.093 €	18.837.000 €
TPM, PRE-ADU & TPM mechanics	496 €	4.464.000 €
		25.914.735 €
TPM, ADU alternative:		
TPM, ADU, 16GBYTE, -2L:	2.426 €	21.831.545 €
		28.909.280 €